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(54) Apparatus for detecting and responding to series arcs in AC electrical systems

(57) Series arcs in an ac circuit (103) are discriminated from other phenomenon by analyzing the timing between pulses (17, 19) in a second derivative (13) of the current signal. A first timer (159) starts timing upon detection of a first pulse (197) in the second derivative of current signal. Time out of the first timer (159) starts a second timer (161) which times a second interval or window during which a series arcing fault will generate a second pulse (19) of opposite polarity to the first pulse. Detection of the first pulse (17) followed by a second pulse (19) of opposite polarity during the window sets a flip-flop (163) to record the event. When a predetermined number of events are counted by a counter (181) within a given time-period set by a third timer (179), an output signal (184) indicating an arcing fault is generated. If the second pulse (19) is generated before the window opens, or a third pulse (43) occurs during the window, the flip-flop (163) cannot be set so that other events such as the switching of a dimmer do not generate a false output signal.

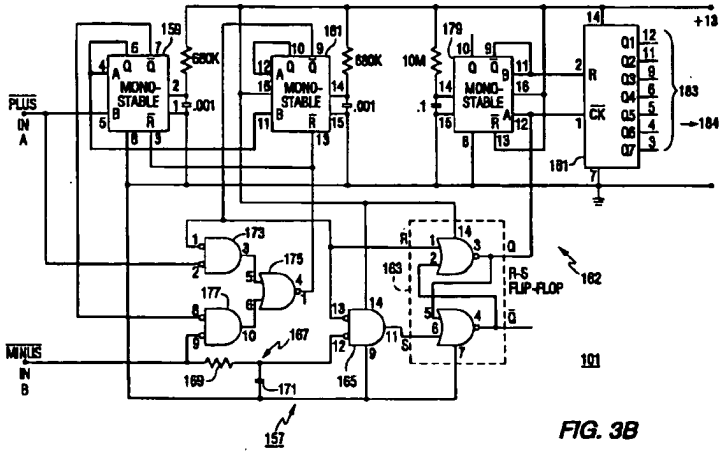

FIG. 3B

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to detection and interruption of series arcs in an ac electrical system.

Background Information

Arcing faults in ac electrical systems are of two types: parallel arcs and series arcs. Parallel arcing faults are line-to-line faults or line-to-ground faults which can occur, for instance, when the insulation on the conductors becomes frayed or is penetrated. Such parallel arcing faults can draw considerable current but usually below the pick-up current or the typical circuit breaker. They also tend to be intermittent because the repulsion forces generated by the current of the arc tends to temporarily separate the conductors and extinguish the arc. Thus, parallel arcs are often referred to as sputtering arcs.

Series arcing faults on the other hand occur in a single conductor path, such as for instance, where a conductor has been cut or at a loose or poor connection. The current in a series arc depends upon the load, but can be in the milliamp range. Previously disclosed methods and apparatus of detecting line-to-line or line-to-ground arcs have proven successful. However, lower level arcs in series with a load may be beyond the capabilities of those techniques. There are two obstacles to merely increasing the sensitivity of prior techniques. At increased sensitivities, there may be more loads and combinations of loads that can produce false trips. Additionally, at lower currents, the current waveform differs from that produced at higher currents, primarily because as the current level will be too low to blow the arc apart, the current will be more continuous, except for discontinuities at current zero crossings. Previous attempts to detect series arcs have primarily focused on analyzing the high frequency content of the arc current. Such techniques typically involve analyzing various figures of merit of this high frequency content. There are several problems with this approach. First, numerous loads, such as for instance computers, have capacitive filters on their inputs while others such as motors or audio equipment with transformer inputs present an inductive impedance to the electrical system. Such loads filter out the high frequency content of the arc current. Furthermore, many of these arc detectors which analyze the high frequency content of the arc current require a microprocessor which increases the cost prohibitively for wide spread use.

There is a need therefore, for an improved apparatus and method for detecting series arcing faults.

There is a further need for such an improved apparatus and method for detecting series arcing faults which can be used in ac circuits powering any of the common types of loads, including loads with capacitive filter inputs, transformers and motor loads.

There is a further need for such series arc detection which can detect such arcs anywhere in the protected circuit portion.

There is an additional need for such series arcing fault detection which operates over a wide dynamic range of fault currents.

There is also a need for providing such an improved apparatus and a method for detecting arcing faults which is economical for wide spread use.

SUMMARY OF THE INVENTION

These needs and others are satisfied by the invention which is based upon the discovery that a series arc generates a recognizable, predictable distortion of the ac current. During each half cycle as the voltage falls below the arc voltage, the current will fall to zero and will remain at zero until the voltage again arises above the arc voltage on the next half cycle. As the arc voltage typically remains constant, the discontinuities in the ac waveform will be repeated regularly at each zero crossing. These discontinuities produce pulses in the second derivative of the current which are of opposite polarity. The sequence of the polarity of the pulses is reversed for zero crossings in the two directions. The two pulses at each zero crossing will be separated in time by the length of the zero crossing discontinuity. This time is a function of the arc voltage, line voltage and line frequency, but is not a linear function of current level. Thus, the technique can be used to detect arcing faults over a wide range of current amplitude.

In accordance with the invention, sensing means are provided to sense the current in the ac circuit and generate a second derivative signal representative of the second derivative of the current. As discussed above, this signal will have pairs of pulses of opposite polarity spaced in time. Thus, means are provided to generate an output signal based upon the timing between pulses of the second derivative signal. More particularly, an output signal indicative of an arcing fault is generated if a second pulse appears in the second derivative of current signal within an interval of predetermined duration commencing a predetermined time after the first pulse and is of opposite polarity to the first pulse.

There are two known loads which may mimic the series arc waveform to some extent. These are a lamp dimmer and a power supply using a full-wave rectifier and a capacitor input filter, as may be used in a television receiver, for example. The power supply can be expected to have a longer discontinuity than a series arc, except for a very short time-period at the turn on of the power supply. Therefore, in accordance with the preferred embodiment of the inventi n, means are provided to generate an output signal indicative of an arc nly when the pattern of a pair of arcs of opposite polarity with the prescribed timing betw en pulses occurs

repeatedly.

The second derivative signal of the current generated by a lamp dimmer has a triple pulse of alternating polarities at each zero crossing. The spacing of the first and second pulses is a function of the dimmer setting, and may, therefore, be within the timing range expected for the series arc. However, the second and third pulses will always be very close together. Therefore, the apparatus in accordance with the invention, includes means which prevent generation of an output signal indicative of an arc if a third pulse follows the second pulse within the interval of predetermined duration. In addition, an additional pulse occurring after the first pulse but before the interval also blocks generation of an output signal.

The invention can include means which detect the polarity sequence of zero crossings in only one direction, or of zero crossings in both directions. In the later case, means can be provided which generate a final output signal only if output signals are generated by means responsive to zero crossings in both directions.

BRIEF DESCRIPTION OF THE DRAWINGS

A full understanding of the invention can be gained from the following description of the preferred embodiments when read in conjunction with the accompanying drawings in which:

Figures 1A, B and C illustrate current, first derivative of current, and second derivative of current waveforms, respectively, generated by a series arc in an electrical system.

Figures 2A, B and C similarly illustrate the current, first derivative of current, and second derivative of current waveforms generated by a dimmer energized by an ac electrical system.

Figures 3A and B are a schematic circuit diagram of a series arc detector in accordance with the invention.

Figure 4 is a schematic block diagram of a modification of a portion of the circuit of Figures 3A and B in accordance of another embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 illustrates waveforms associated with a series arc in an ac electrical system. The trace 1 in Figure 1A illustrates the current. When the voltage in the ac system falls below the arcing voltage (typically about 20 to 30 volts in a 120 volt system) the current is interrupted as at 3 in Figure 1A. The current remains at 0 until the voltage rises above the arcing voltage on the next half-cycle and the arc is restruck. Thus, at the point 5, following reestablishment of the arc, the current is reestablished.

The first derivative of the arcing current 1 shown in Figure 1A is illustrated in Figure 1B as the trace 7. As can be se n, there are substantial st ps 9 and 11 when the current is interrupted and when it is again reestablished. Figure 1C illustrates the second derivative 13 of the arcing current. The second derivative signal 13 exhibits a pair 15 of pulses 17 and 19 resulting from the discontinuities in the current at the interruption of the arc and the reestablishment of the arc. It can be seen that these pulses 17 and 19 are of opposite polarity. As can also be seen, the polarity sequence is dependent upon the direction of the zero crossing. In other words, the polarity sequence is reversed on successive half cycles.

As mentioned above, a load that can generate waveforms having a similarity to those generated by a series arc is a dimmer. A dimmer delays turn-on of a switching device during each half-cycle of ac voltage in order to control power delivered to the load. Typically, the phase-back angle is selectable to provide a range of power settings. This delayed switching produces the waveforms illustrated in Figures 2A, B, and C. Figure 2A illustrates the dimmer current waveform 21. As can be seen, the current is turned off at 23 at the end of a half-cycle and remains at zero until the dimmer switch again turns on at 25, causing the current to increase rapidly to the point 27 where it then becomes sinusoidal. Figure 2B illustrates the first derivative 29 of the dimmer current. As can be seen, it has a discontinuity at 31 where its value goes to zero and a spike at 33. Figure 2C illustrates the second derivative waveform 35 of the dimmer current. As can be seen, this second derivative of dimmer current has a small pulse 37 where the current falls to 0 and then remains at 0, and a pair of pulses 39 which includes a first pulse 41 when the current first reestablishes and increases rapidly, and a second pulse 43 where the current transitions to a sinusoidal waveform. As illustrated, the pulses 41 and 43 are of opposite polarity. It can also be seen that the pulses 37 and 41 are of opposite polarity.

The technique for series arc detection of the invention takes advantage of the fact that the second pulse 19 in the second derivative of the current resulting from a series arcing fault follows the first pulse 17 by a predictable interval of time and is of opposite polarity. Hence, such a pulse can be detected by looking for a second pulse in the second derivative current of the ac electrical system which occurs within a time window commencing a selected time after a first pulse and is of opposite polarity to the first pulse. Referring to Figure 2C, it can be seen that the dimmer generates a pair of pulses 37 and 41 which are spaced in time and of opposite polarity. The pulses 41 and 43 also constitute a pair of pulses of opposite polarity but they are always in rapid succession. It is possible, however for the timing between the pulses 37 and 41 to fall within the window established for detecting the pulses 17 and 19. In order to discriminate the series arcing fault from a dimmer, the present invention looks for the third puls 43 which rapidly follows the second pulse 41 in the second derivative of the dimmer current. It also ign res conditions in which the second pulse follows the first pulse too

quickly.

Figures 3A and B illustrate an exemplary embodiment of the arcing fault detector 101 in accordance with the inv ntion for detecting series arcing faults in an ac electrical system 103 having one conductor 105 which may be the line or neutral conductor. A sensing circuit 107 senses the second derivative of current flowing in the conductor 105. This sensing circuit 107 includes a current transformer 109 which generates a first derivative of current signal, di/dt, through use of a core of material such as powdered iron which has a low mu and a high flux saturation level. This first derivative of current signal, di/dt is bandwidth limited by bandwidth limiter 111 comprising a shunt capacitor 113 and resistor 115. A differentiator 117 in the form of series capacitor 119 and resistor 121 generates a second derivative of current signal di^2/dt. Additional bandwidth limiting is provided by the circuit 123 which includes an op amp 125 with feedback resistor 127 and feedback capacitor 129. The zener diodes 131 prevent saturation of the op amp 125 by large pulses in the di^2/dt signal. Further attenuation of 60 Hz noise is provided by the capacitor 133. RF noise suppression is provided by the capacitor 135 across the inputs to the op amp 125.

As the pulses on the di^2/dt signal can have a wide dynamic range, an amplifier stage 137 comprising the op amp 139 with feedback resistor 141, and input resistor 143 is provided. Again, back-to-back zener diodes 145 prevent the op amp 139 from saturating on large pulses and the capacitor 147 provides RF noise suppression.

The sensing circuit 107 also includes differential comparators 149 and 151 which compare the output of the amplifier stage 137 to reference voltages of 6.5 volts and 19.5 volts respectively. As a plus 13 volt bias is applied to the op amps 125 and 139, the signal applied to the non-inverting input of the comparator 49 and to the inverting input of the comparator 51 are 13 volts when the di^2/dt signal is zero. Under these conditions the outputs of the comparators 149 and 151 are high and the MINUSBAR OUT signal at the output of the comparator 149 is pulled up to 13 volts by the pull-up resistor 153. Similarly, the PLUSBAR OUT output signal of the comparator 151 is pulled up to 13 volts by the pull-up a resistor 155. A positive pulse in the di^2/dt signal at the output of the op amp 139 which is above an absolute threshold of 6.5 volts causes the PLUSBAR OUT signal to go low. A negative pulse of more than 6.5 volts absolute similarly causes the MINUSBAR OUT signal to go low. Thus, the PLUSBAR OUT and MINUSBAR OUT signals are normally high, but go low momentarily in response to a positive and negative pulse, respectively, in the di^2/dt signal.

Figure 3B illustrates a signal generating circuit 157 which generates an output signal indicative of an arc in resp nse to a preselected polarity sequence and timing betw en pulses in the di^2/dt. Th PLUSBAR signal is applied to the B input of a first monostable 159. The negative or trailing edge of the PLUSBAR signal initiates timing by the monostable 159 of the first timing interval. This causes the Q output of the monostabl 159 to go high. When monostable 159 times out, its Q output goes low triggering a second monostable 161 to begin timing the second timing interval. This is th timing interval in which a second pulse of opposite polarity will appear in the case of a series arcing fault.

An output signal generator 162 includes an R-S flip-flop 163 which has the QBAR output of the second monostable 161 connected to its reset input R. As the QBAR output of monostable 61 is normally high except during the second timing interval the Q output of the R-S flip-flop will normally be low. The S input of the R-S flip-flop 163 is connected to a negative logic NAND circuit 165 having as one input the QBAR output of the second monostable 161 and the MINUSBAR signal applied through a delay circuit 167 which includes a series resistor 169 and shunt capacitor 171. The negative logic NAND element 165 is only enabled by the QBAR output of the second monostable 161 during the second timing interval. A negative pulse in the di^2/dt signal (MINUSBAR goes low) during this second timing interval will cause the S input to the R-S flip-flop 163 to go high setting the Q output of the flip-flop high. The delay 167 prevents the flip-flop 163 from being set until it is determined that a third pulse does not occur during the second interval. This condition is detected by circuitry which includes a having as one input the PLUSBAR signal and as the other input the QBAR output of the second monostable 161. Thus, during the second interval the output of negative logic NAND element 173 logic NAND at 173 will normally be zero. This output of the negative logic NAND 173 serves as an input to a NOR element 175 which has as a second input the output of a negative logic NAND circuit 77 which, as will be explained, is low during the second interval. Thus, normally during a second interval the output of a NOR 175 will be high which maintains the RBAR inputs to the first and second monostables 159 and 161 high. If the PLUSBAR signal goes low during the second interval, indicating a second pulse during the second interval or a third pulse since timing began, the output of the negative logic NAND 173 goes high which makes the output of NOR 175 to go low, thereby resetting both monostables 159 and 161. When the second monostable 161 is reset, its QBAR signal goes high to reset the R-S flip-flop 163 and disabling the negative logic NAND 165 to prevent the MINUSBAR signal from setting the R-S flip-flop after the time delay 167 is timed out.

The negative logic NAND 177 terminates timing if the second pulse, MINUSBAR, occurs too early, that is during the first interval. During this first interval, the negative logic NAND 177 is enabled by the QBAR signal from the first monostable 159. Normally, the MINUSBAR signal is high during the first interval thereby causing the output of negative logic NAND 177 to be low. However, if the MINUSBAR signal goes low, indicating a second pulse in the di^2/dt signal, the output of the negative logic NAND 177 goes high thereby resetting the

monostables 159 and 161 through the NOR 175.

When the Q output of the R-S flip-flop 163 goes high signifying detection of a positive pulse followed by a negative pulse within a time interval (the second time interval) commencing a predetermined time (the first time interval) after the first pulse, a third monostable 179 which forms part of the output signal generator 162 begins counting a time interval. This output of the R-S flop-flop 163 also clocks a digital timer 181. Each time the R-S flop-flop 163 generates a pulse during the time interval set by the monostable 179 the counter 181 is incremented. When the monostable 179 times out, its QBAR output goes high to reset the counter 181. A selected one of the outputs 183 of the counter 181 provides the output signal 184 indicative of an arcing fault. The selected output count indicates the number of events in which a positive pulse was followed by a negative pulse during a time interval set by the monostable 179.

The circuit of Figures 2A and 2B only counts events in which a positive pulse in the di^2/dt signal is followed by a negative pulse within a given time interval. Thus, it only counts such events which occur during negative-to-positive zero crossings, or one time per cycle. By reversing the PLUSBAR and MINUSBAR inputs in Figure 2B, events occurring on the opposite direction zero crossings could be detected. Again, this would only count one event per cycle of the ac cycle. In order to increase the reliability of the series arcing detector, the pulses of opposite polarity in the di^2/dt signal during each half cycle can be detected. This could be accomplished by duplicating the circuit of Figure 2B with the PLUSBAR and MINUSBAR inputs reversed with the outputs of the respective R-S flip-flops connected to a common timer 179 and digital counter 181. A simpler arrangement is to provide a reversing circuit 185 as shown in Figure 3. This reversing circuit 185 includes four CMOS switches 187, 189, 191, and 193. The switch 187 connects the PLUSBAR signals to an output A while the switch 189 connects the same signal to the output B. Similarly, the switch 191 connects the MINUSBAR signal to the A output while the switch 193 connects it to the B output. The switches 187 and 193 are simultaneously closed by a high output on the Q_1 output of the counter 81 so when this count is high the PLUSBAR signal is connected to the A output and the MINUSBAR signal is connected to the B output. An inverter 195 turns on the switches 189 and 191 to reverse the PLUSBAR and MINUSBAR signals on alternate counts of the counter. As these outputs A and B are connected to the A and B inputs of signal generating circuit 157 in Figure 3B, it can be appreciated that events occurring at both zero crossings of the ac current are detected. In this case, the count on the digital counter 181 during the interval determined by the monostable 179 would be doubled that described in the first instance wher only events occurring at zero crossings in on direction were counted.

The series arcing detector of this invention can be used by itself to provide an indication of a series arc. It can also be incorporated into a circuit breaker to provide a trip signal in r sponse to the series arc. Furthermore, it could be used in conjuncti n with a parallel arcing fault detector such as that disclosed in U.S. patent number 5,224,006.

While specific embodiments of the invention have been described in detail, it will be appreciated by those skilled in the art that various modifications and alternatives to those details could be developed in light of the overall teachings of the disclosure. Accordingly, the particular arrangements disclosed are meant to be illustrative only and not limiting as to the scope of invention which is to be given the full breadth of the claims appended and any and all equivalents thereof.

Claims

1. Apparatus (101) for detecting a series arcing fault in an ac circuit (103), said apparatus comprising:

   sensing means (107) sensing a second derivative of ac current (1) in said ac circuit (103) to generate a second derivative signal (13) containing pulses (15) in response to discontinuities in said ac current such as said series arcing fault; and

   signal generating means (157) generating an output signal (184) indicative of said series arcing fault in response to predetermined timing between said pulses (15) in said second derivative signal (13).

2. The apparatus (101) of Claim 1 wherein said sensing means (107) generates from said second derivative signal (13) a signal containing pairs of pulses (15) with a second pulse (19) occurring during an interval of predetermined duration commencing a predetermined time after a first pulse (17), and wherein said signal generating means (157) comprises means (162) generating said output signal only when said second pulse (19) occurs within said second interval after said first pulse (17).

3. The apparatus (1) of Claim 2 wherein said signal generating means (157) comprises means (171, 175, 177) preventing generation of said output signal if an additional pulse occurs in said second derivative signal (13) in said interval.

4. The apparatus (101) of Claim 3 wherein said means (171, 177) preventing generation of said output includes means (171) delaying said means (162) generating said output signal until additional means (177) determine that no additional signal has occurred in said interval.

5. The apparatus (101) of Claim 3 wherein said signal generating means (157) further includes means

(173, 175) preventing generation of said output signal if said second pulse (19) occurs before said interval.

6. The apparatus (101) of Claim 2 wherein said signal generating means (157) comprises means (173, 175) preventing generation of said output signal if said second pulse (19) occurs before said interval.

7. The apparatus (101) of Claim 2 wherein said sensing means (107) generating said second derivative signal with pulses, generates first (17) and second (19) pulses of opposite polarity in response to a series arcing fault, and wherein said means (162) generating said output signal comprises means (163, 165) only generating an output signal when said second pulse (19) occurs within said interval and is of opposite polarity to said first pulse (17).

8. The apparatus (101) of Claim 7 wherein said means (163, 165) generating said output signal only when said first pulse is of a first polarity and said second pulse is of opposite polarity.

9. The apparatus (101) of Claim 7 wherein said signal generating means (157) includes means (173, 175, 177) preventing said means (162) generating said output signal from generating said output signal when an additional pulse (19, 43) of either polarity occurs after said first pulse (17) and before said interval.

10. The apparatus (101) of Claim 7 wherein said signal generating means (157) comprises first means (157, 187, 193) generating a first event signal when said first pulse (17) is of first polarity and said second pulse (19) of a second polarity opposite said first polarity occurs within said interval, and second means (157, 189, 191) generating a second event signal when said first pulse (19) is of said second polarity and said second pulse (19) of said first polarity occurs within said interval and wherein said output means (162) generates an output signal only when a predetermined number of said first and second event signals occur within a given time period.

11. The apparatus (101) of Claim 7 wherein said means (162) generating said output signal includes means (181) generating a count of said first and second event signals and means (179) generating said output signal only when said count reaches a predetermined number within a given time period.

12. The apparatus (101) of Claim 1 wherein said signal generating means (157) includes means (181) generating a count of times that said second pulse (19) occurs during said interval after said first pulse (17) and means (179) generating said output signal only wh n said count reaches a predetermined count within a given time period.

13. A method of detecting series arcing faults in and ac circuit (103) comprising the steps of:

generating a second derivative signal (13) representative of a second derivative of current flowing in said ac circuit (103) and having pulses (17, 19) in response to discontinuities in said current such as in arcing fault;
measuring time between pulses (17, 19) in said second derivative signal (13); and
generating an output signal (184) indicative of an arcing fault in response to predetermined timing between said pulses (17, 19).

14. The method of Claim 13 wherein said step generating an output signal (1840 comprises generating said output signal only when said second pulse (19) occurs during an interval of predetermined duration commencing within a predetermined time period after a first pulse (17).

15. The method of Claim 14 wherein said step of generating said output signal (184) comprises generating said output signal only when said second pulse (19) is of opposite polarity to said first pulse (17).

16. The method of Claim 14 wherein said step of generating said output signal (184) includes not generating an output signal if a third pulse (43) occurs during said interval.

17. The method of Claim 14 wherein said step of generating said output signal (184) includes not generating said output signal when said second pulse (19) occurs after said first pulse (19) but before said interval.

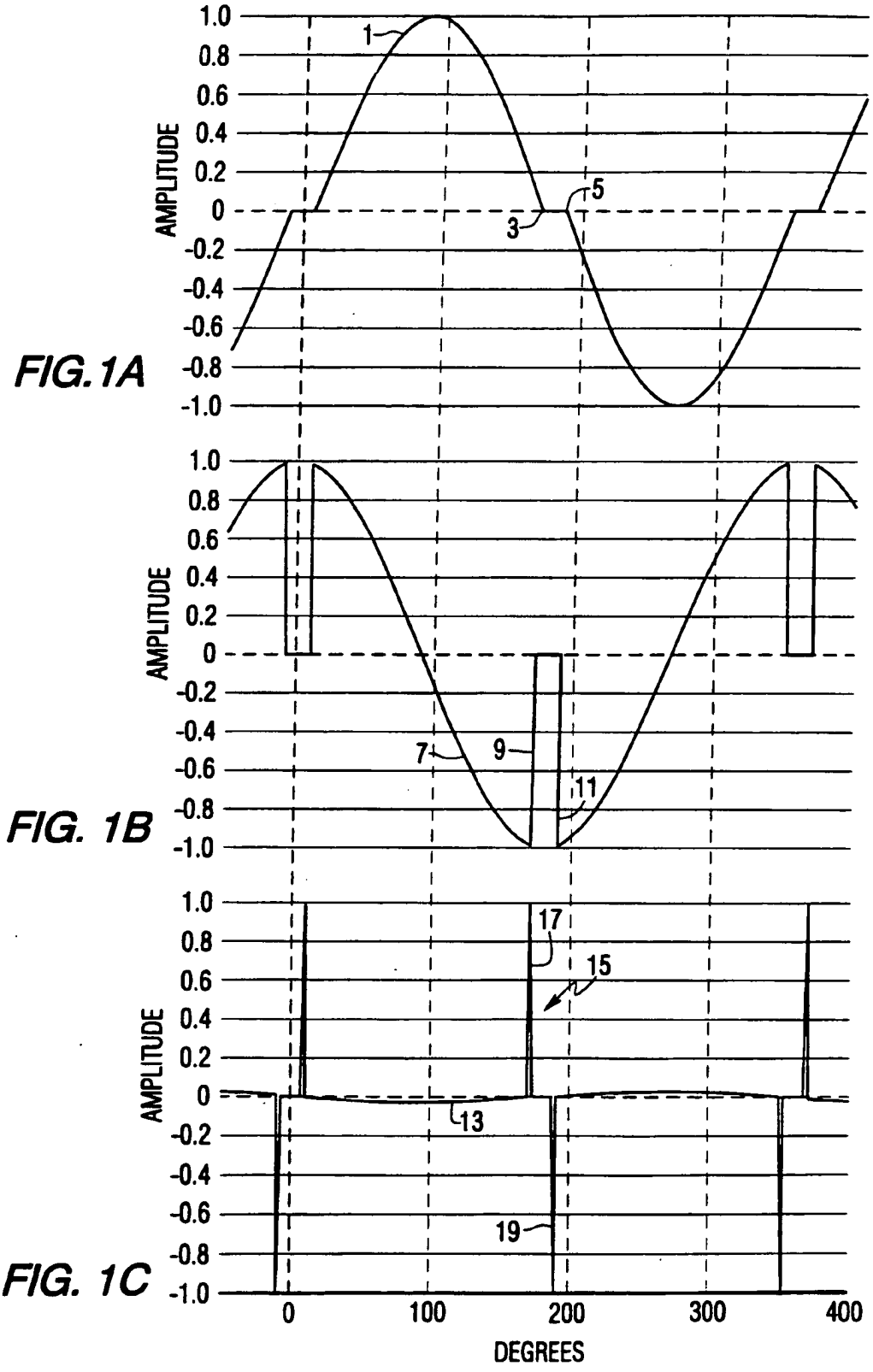


FIG. 1A

FIG. 1B

FIG. 1C

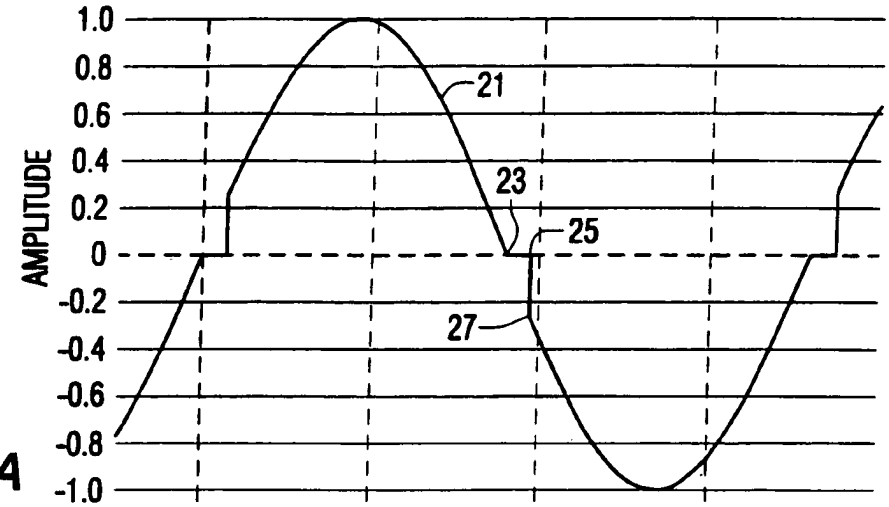


FIG. 2A

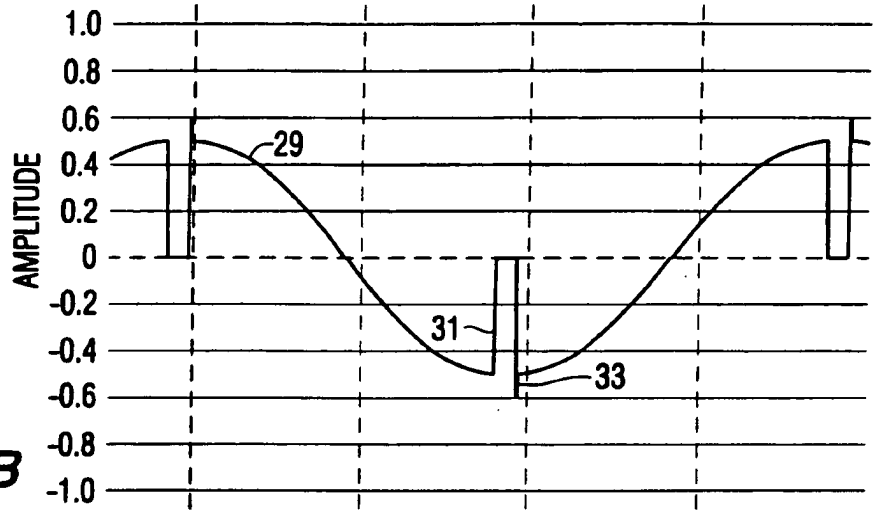


FIG. 2B

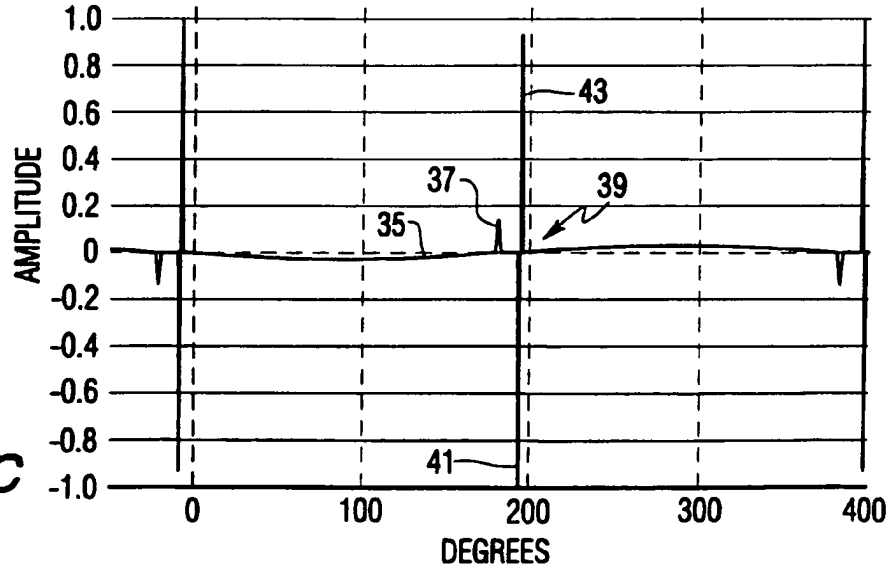
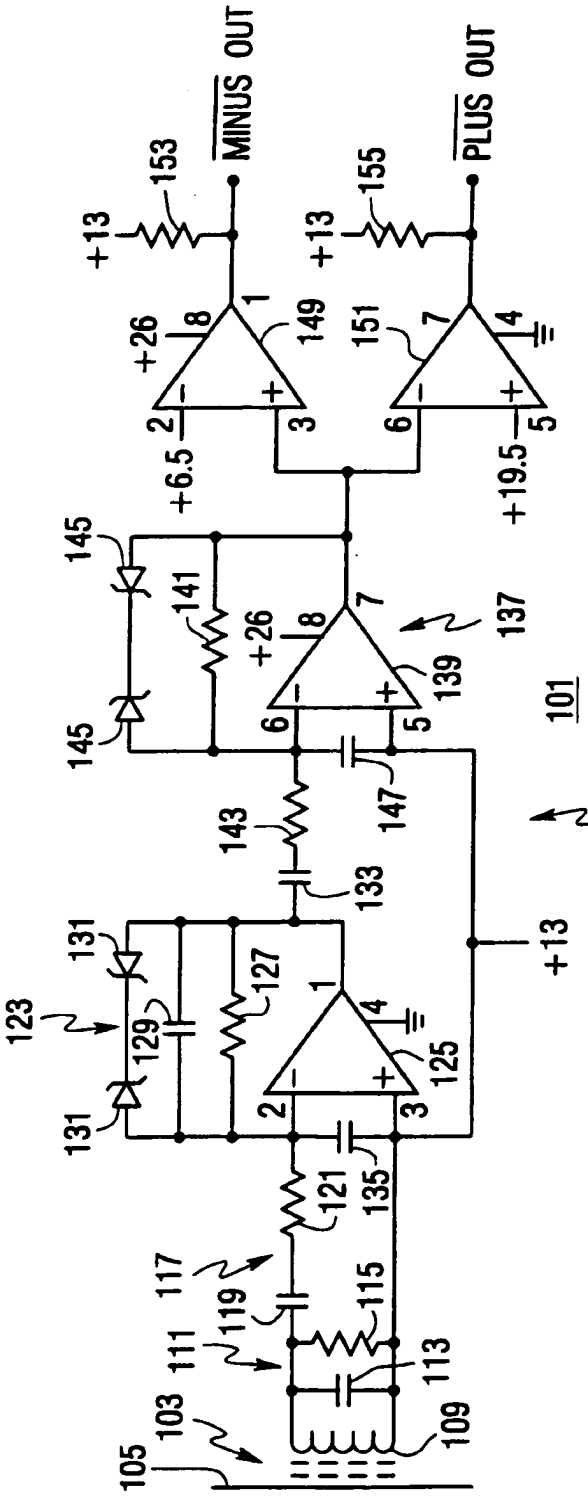


FIG. 2C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PLUS OUT
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+26
+6.5
+19.5
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143
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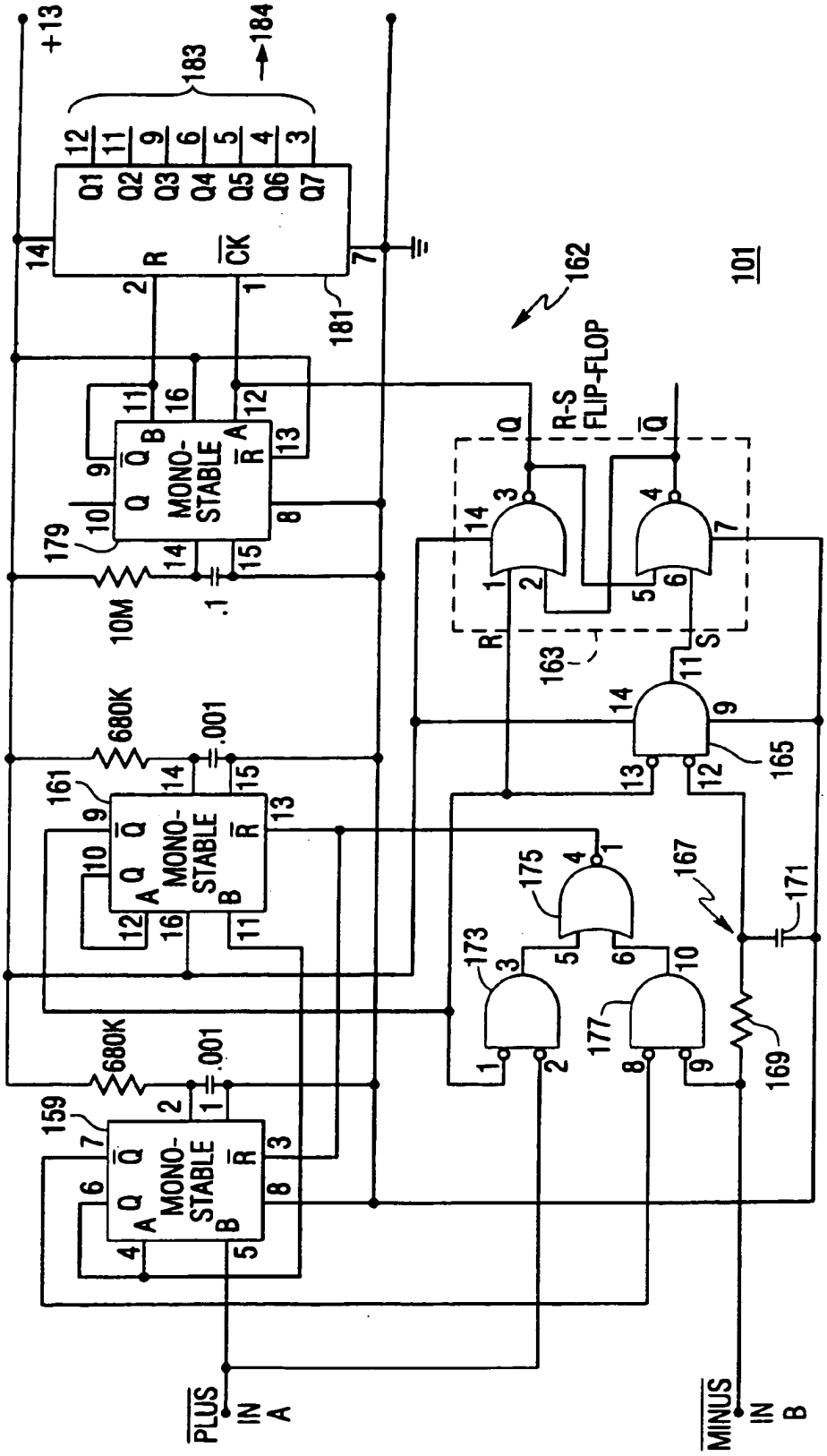
101
107

FIG. 3A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184
Q1
Q2
Q3
Q4
Q5
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Q7
R
CK
181
162
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FLIP-FLOP
MONO-
STABLE
179
10M
.1
680K
.001
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165
167
169
171
173
175
177
157
PLUS
IN
A
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FIG. 3B

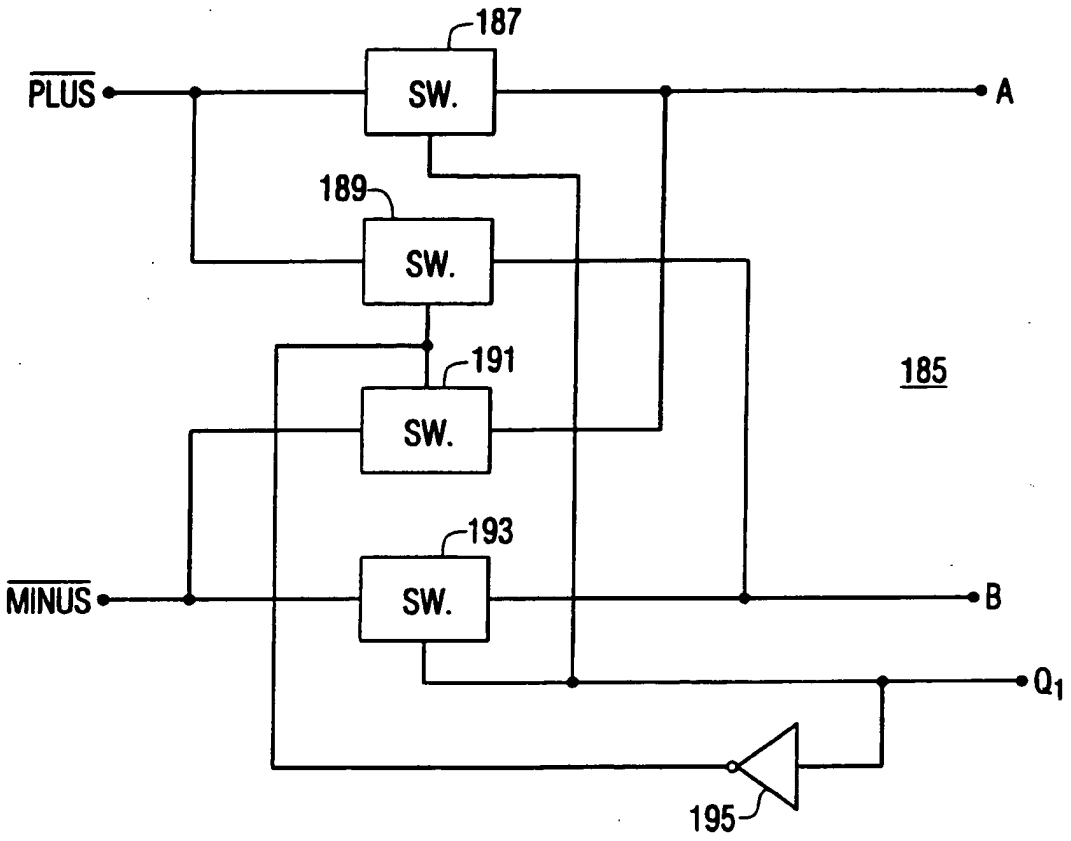

FIG. 4